



# CMT4001AHPQ

40V N-Channel Power MOSFET

## Product Summary

$V_{DS}$	$R_{DS(ON)_{MAX}}$	$I_{D\_MAX}$
40 V	1.4 m $\Omega$ @ $V_{GS} = 10V$	223 A

## Sinesemi Automotive MOSFET



## Features

- N-Channel Enhancement Mode - Standard Level
- AEC-Q101 Qualified, PPAP Capable
- 175°C Operating Temperature
- 100%  $\Delta V_{DS}$  & UIS &  $R_g$  Tested

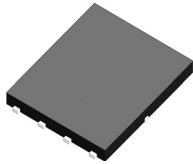
## Applications

- General Automotive Applications

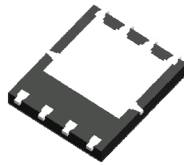
## Mechanical Data

- Green Molding Compound
- Moisture Sensitivity: Level 1 per J-STD-020
- UL Flammability Classification Rating 94V-0

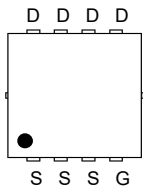
## PDFN5060-8L



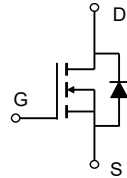
Top View



Bottom View



PIN Configuration  
(Top View)



Schematic Diagram

## Ordering Information

Orderable Part Number	Package Type	Device Marking	Form	Quantity (pcs)
CMT4001AHPQ	PDFN5060-8L	4001AHQ	13" Tape&Reel	5,000

## Maximum Ratings (@ $T_C = 25^\circ\text{C}$ , unless otherwise specified.)

Parameter	Symbol	Value	Unit
Drain - Source Voltage	$V_{DS}$	40	V
Gate - Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $V_{GS} = 10V$ ) <sup>(1)</sup>	$I_D$	$T_C = 25^\circ\text{C}$	223
		$T_C = 100^\circ\text{C}$	158
Pulsed Drain Current <sup>(2)</sup>	$I_{DM}$	893	A
Single Pulse Avalanche Energy <sup>(3)</sup>	$E_{AS}$	436	mJ
Single Pulse Avalanche Current ( $L = 0.1\text{mH}$ )	$I_{AS}$	56	A
Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	125
		$T_C = 100^\circ\text{C}$	63
Junction & Storage Temperature Range	$T_J, T_{STG}$	-55 ~ +175	$^\circ\text{C}$

## Thermal Characteristics

Parameter	Symbol	Typ.	Max.	Unit
Thermal Resistance, Junction-to-Ambient <sup>(4)</sup>	$R_{\theta JA}$	35	45	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case <sup>(5)</sup>	$R_{\theta JC}$	0.9	1.2	$^\circ\text{C/W}$



**Electrical Characteristics** (@  $T_J = 25^\circ\text{C}$ , unless otherwise specified.)

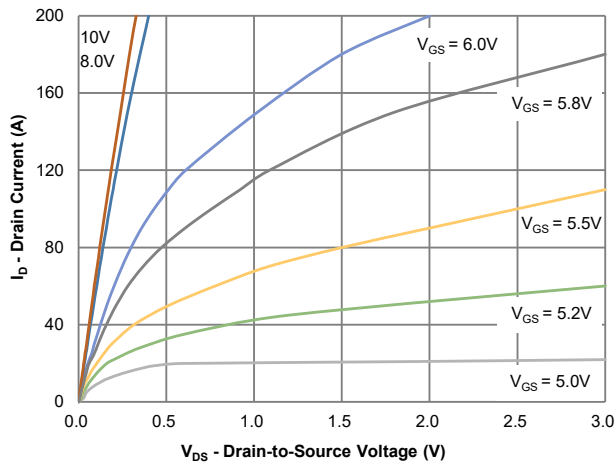
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Off Characteristics <sup>(6)</sup></b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40V, V_{GS} = 0V$ $T_J = 125^\circ\text{C}$	-	-	1.0	$\mu A$
			-	-	100	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	$\pm 100$	nA
<b>On Characteristics <sup>(6)</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 20A$	-	1.2	1.4	m $\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 5.0V, I_D = 20A$	-	34	-	S
Diodes Forward Voltage	$V_{SD}$	$I_S = 2.0A, V_{GS} = 0V$	-	0.7	1.2	V
<b>Dynamic Characteristics <sup>(7)</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 20V, V_{GS} = 0V, f = 1\text{MHz}$	-	3073	-	pF
Output Capacitance	$C_{oss}$		-	1515	-	pF
Reverse Transfer Capacitance	$C_{rss}$		-	58	-	pF
Gate Resistance	$R_g$	$V_{GS} = 0V, V_{DS} = 0V, f = 1\text{MHz}$	-	1.4	-	$\Omega$
<b>Switching Characteristics <sup>(7)</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DS} = 20V$ $I_D = 20A, R_{GEN} = 3.0\Omega$	-	5.6	-	ns
Rise Time	$t_r$		-	15	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	20	-	ns
Fall Time	$t_f$		-	9.9	-	ns
<b>Gate Charge Characteristics <sup>(7)</sup></b>						
Total Gate Charge ( $V_{GS} = 10V$ )	$Q_g$	$V_{DS} = 20V, I_D = 20A$ $V_{GS} = 10V$	-	41	-	nC
Total Gate Charge ( $V_{GS} = 6.0V$ )	$Q_g$		-	26	-	nC
Gate-Source Charge	$Q_{gs}$		-	14	-	nC
Gate-Drain Charge	$Q_{gd}$		-	7.5	-	nC
Gate Plateau Voltage	$V_{plateau}$		-	5.0	-	V
<b>Drain-Source Diode Characteristics <sup>(7)</sup></b>						
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 20A, dI/dt = 100A/\mu s,$ $T_J = 25^\circ\text{C}$	-	46	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	50	-	nC
Diode Forward Current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	132	A

**Notes:**

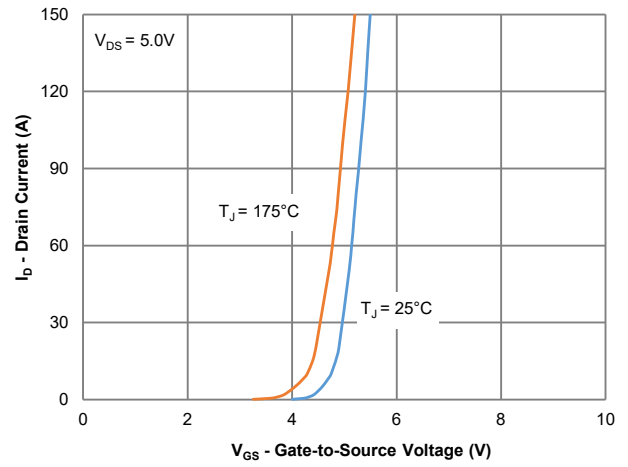
1. This current is chip limited, which is calculated based on  $R_{thjc}$ .
2. This current is calculated on single pulse with 10 $\mu s$  Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test,  $E_{AS}$  condition:  $T_J = 25^\circ\text{C}, V_{DD} = 20V, V_{GS} = 10V, L = 1.0\text{mH}$ .
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to soldering point (on the exposed drain pad).
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.



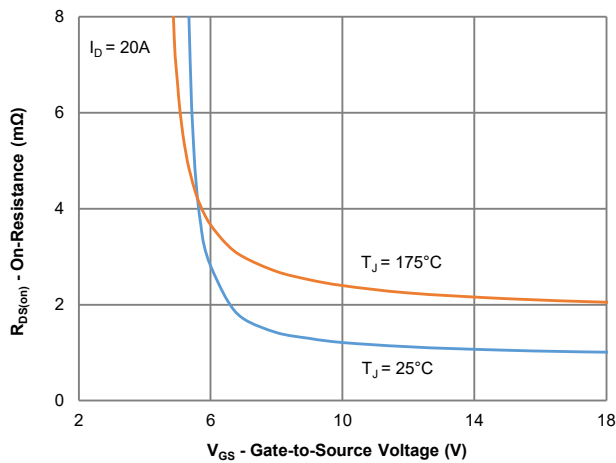
**Typical Electrical and Thermal Characteristics**



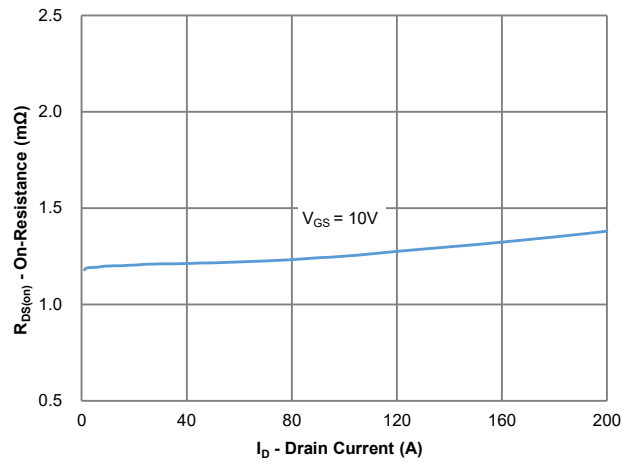
**Figure 1: Output Characteristics**



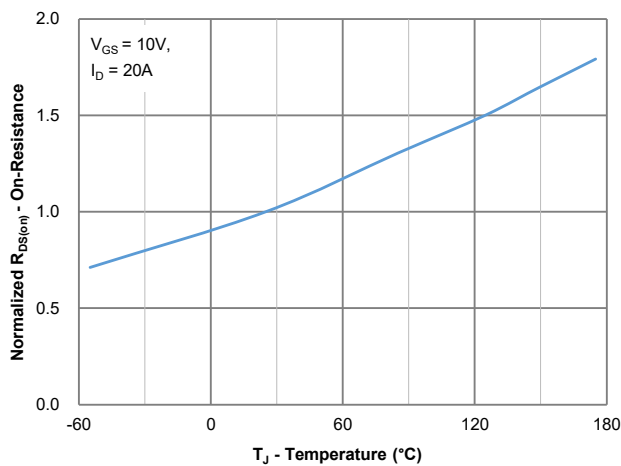
**Figure 2: Transfer Characteristics**



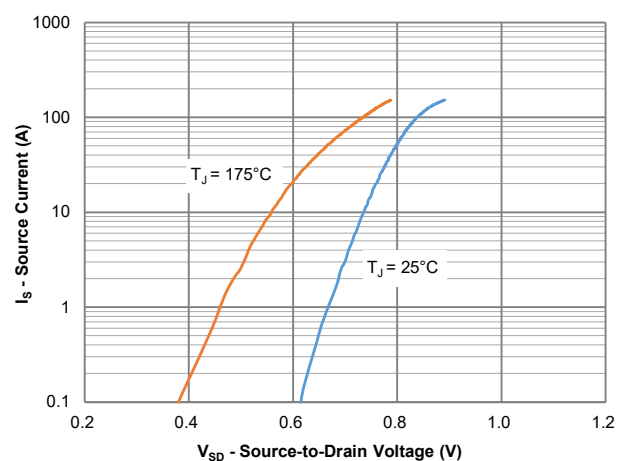
**Figure 3: On-Resistance vs. Gate-Source Voltage**



**Figure 4: On-Resistance vs. Drain Current**



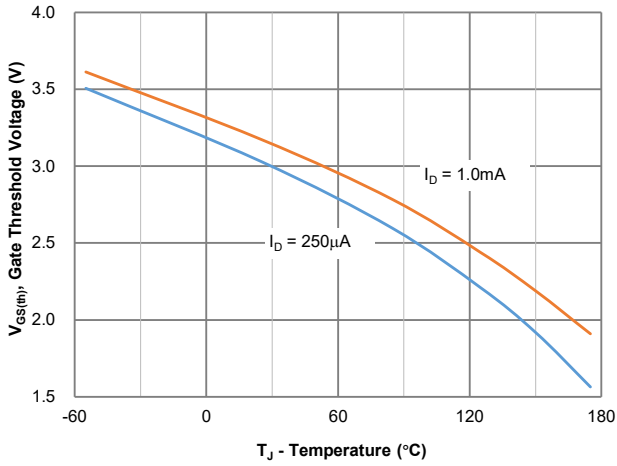
**Figure 5: On-Resistance vs. Junction Temperature**



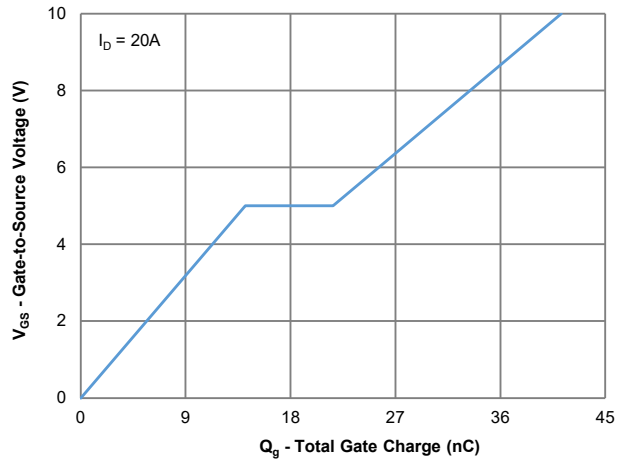
**Figure 6: Source-Drain Diode Forward Voltage**



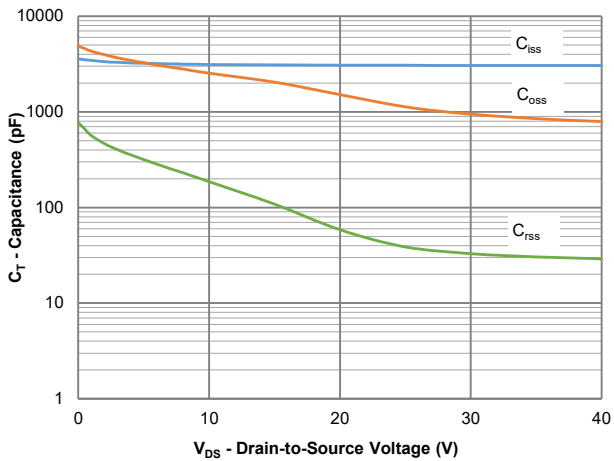
**Typical Electrical and Thermal Characteristics**



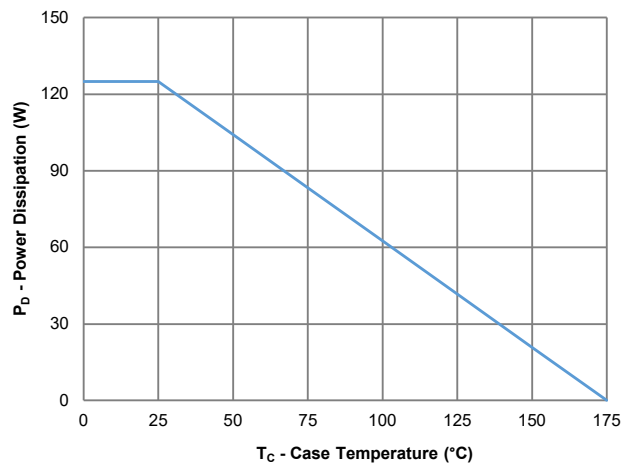
**Figure 7: Gate Threshold Variation vs. Junction Temperature**



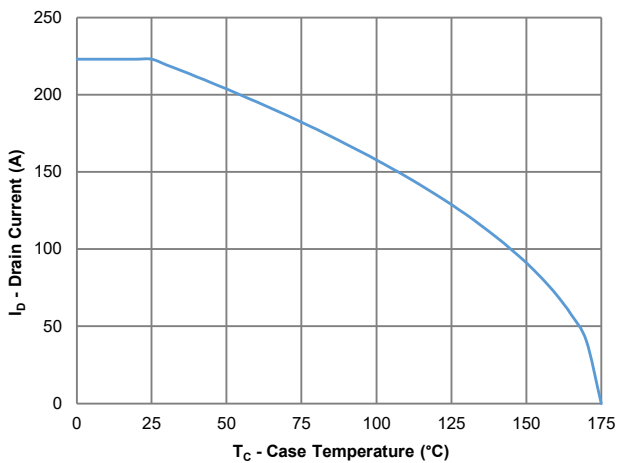
**Figure 8: Gate Charge Characteristics**



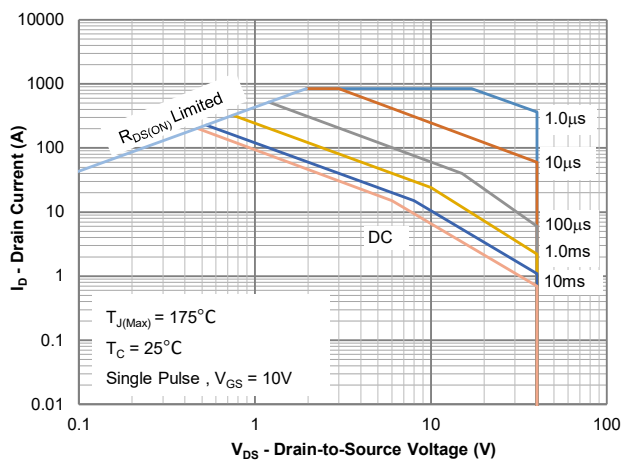
**Figure 9: Capacitance Characteristics**



**Figure 10: Power Derating**



**Figure 11: Current Derating**



**Figure 12: Safe Operating Area**



Typical Electrical and Thermal Characteristics

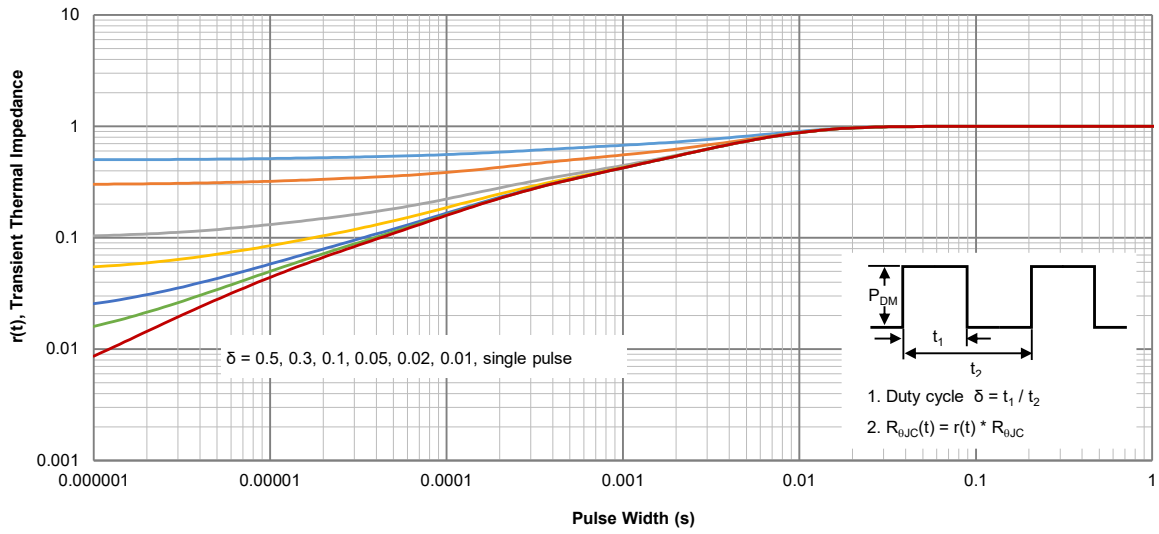
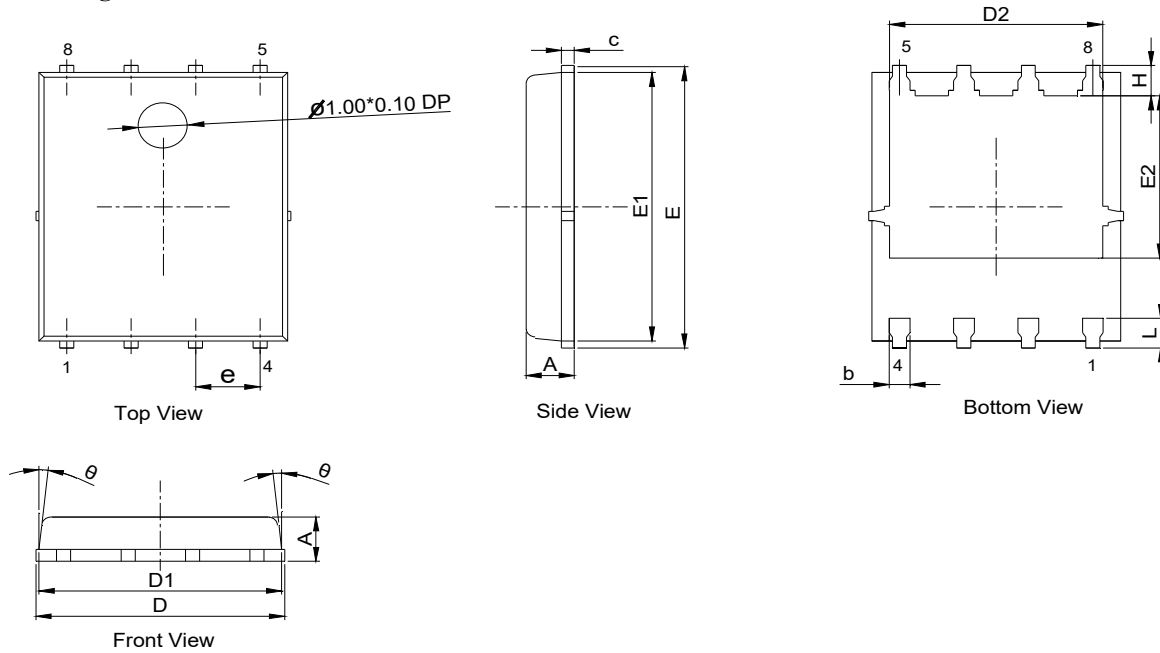


Figure 13: Normalized Maximum Transient Thermal Impedance



PDFN5060-8L Package Outline

Package Outline

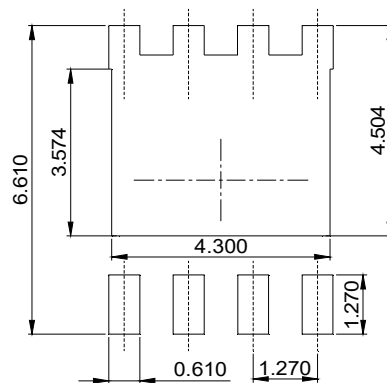


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.30	0.41	0.51
c	0.20	0.25	0.34
D	4.80	--	5.40
D1	4.65	--	5.30
D2	3.60	--	4.25
E	5.90	--	6.50
E1	5.70	--	6.00
E2	3.38	--	3.92
e	1.27BSC		
H	0.40	--	0.93
L	0.40	--	0.91
$\theta$	0°	--	12°

Recommended Soldering Footprint



DIMENSIONS: MILLIMETERS